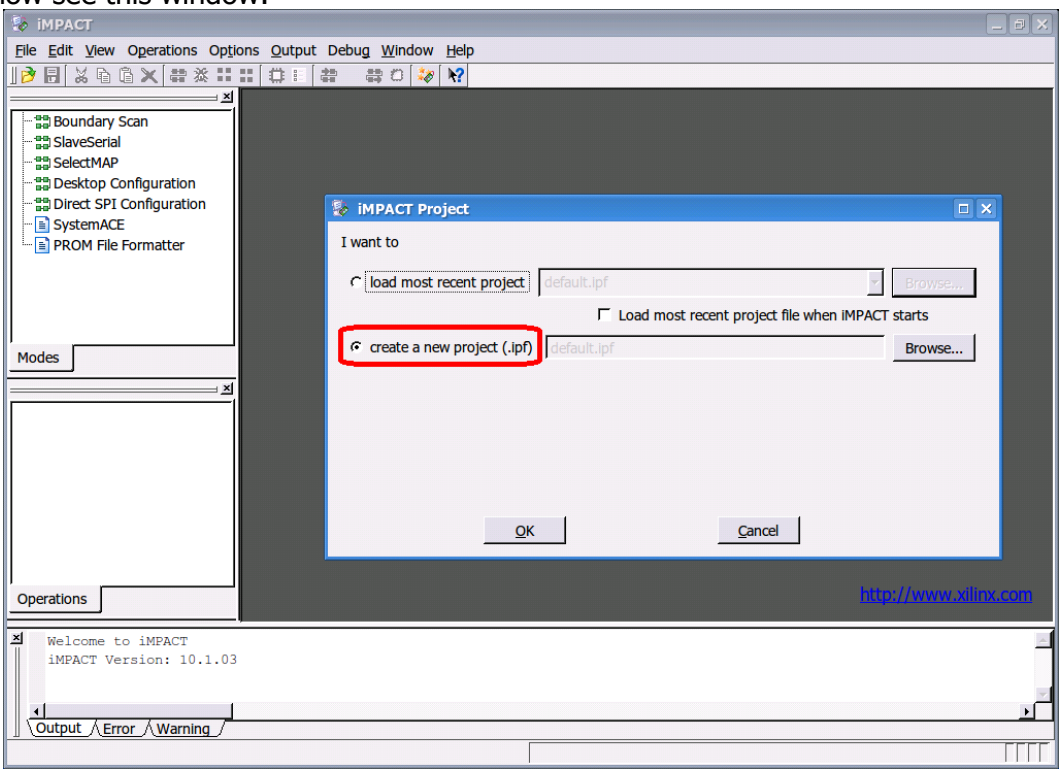
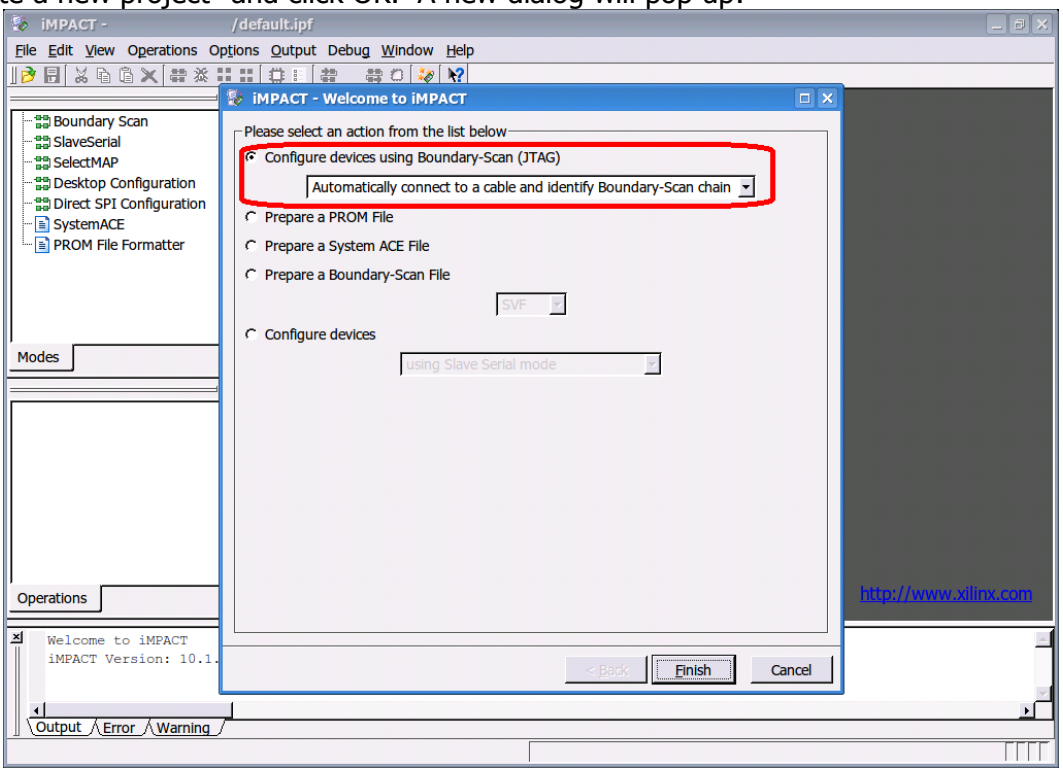
HOW TO CREATE A NEW XILINX IMPACT PROJECT FOR THE RAPTOR ENGINEERING VDFPGA BOARD

1. Launch Xilinx iMPACT 10.1 or above. If a warning message pops up, ignore it and click OK.

   You should now see this window:

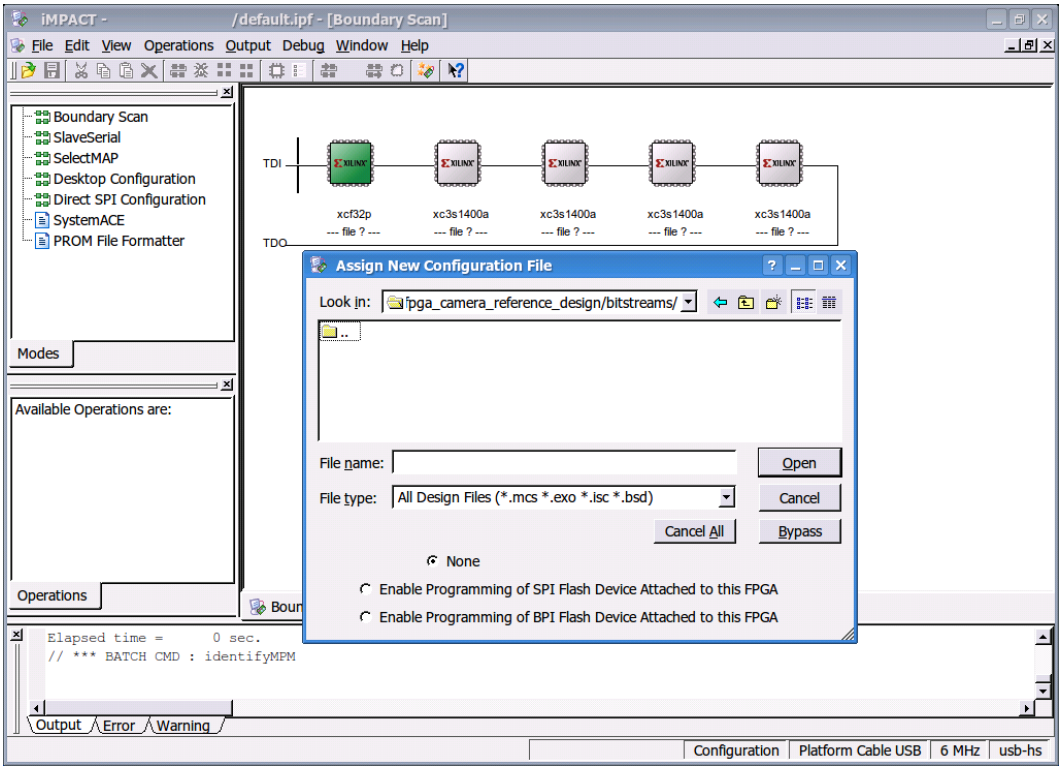


2. Select "create a new project" and click OK. A new dialog will pop up:



3. Make sure the highlighted options are selected and click "Finish".

You will now be prompted for the location of the configuration files for each device on the board, starting with the FLASH PROM:

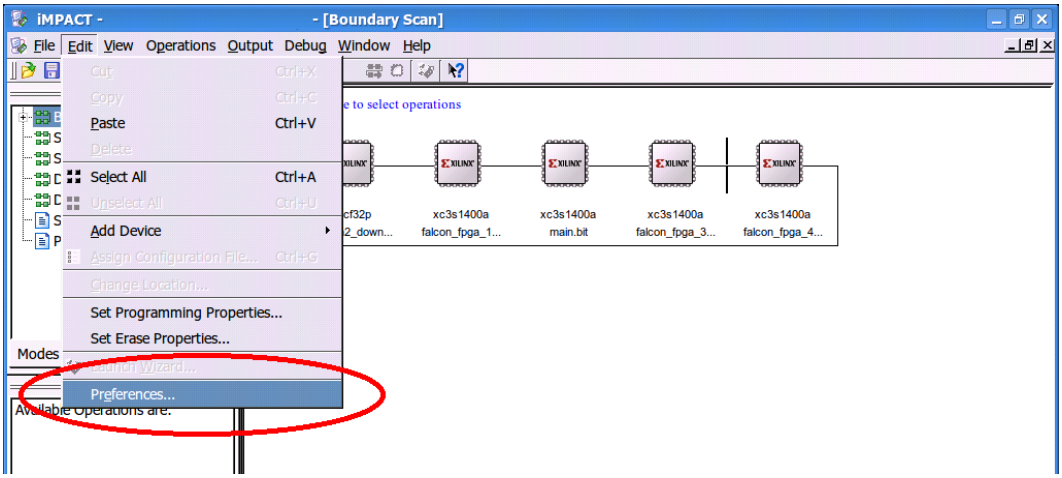


The currently selected device is shown in green. The default configuration files are available in the folders vdfpga_camera_reference_design/ and vdfpga_camera_reference_design/bitstreams/

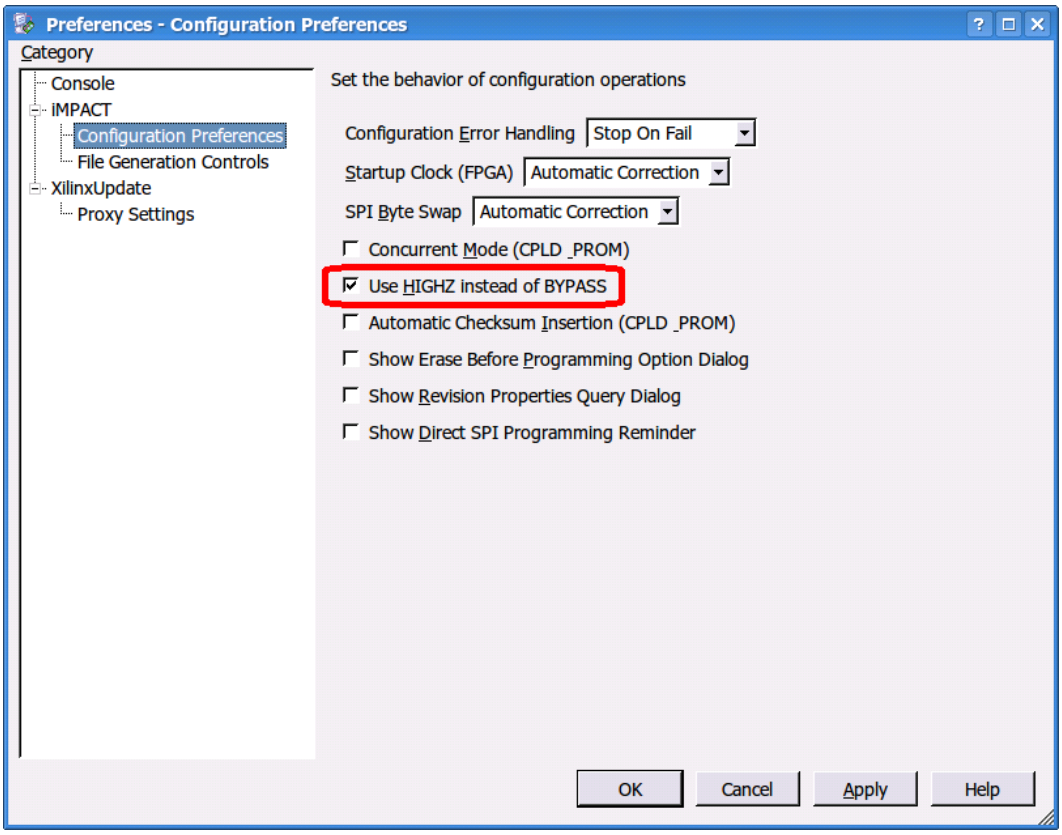
4. You will need to give iMPACT the configuration files in the following sequence:
    1. [FLASH PROM] vdfpga_camera_reference_design/falcon2_download.mcs
    2. [FPGA 1] vdfpga_camera_reference_design/bitstreams/falcon_fpga_1.bit
    3. [FPGA 2] vdfpga_camera_reference_design/bitstreams/falcon_fpga_2.bit
    4. [FPGA 3] vdfpga_camera_reference_design/bitstreams/falcon_fpga_3.bit
    5. [FPGA 4] vdfpga_camera_reference_design/bitstreams/falcon_fpga_4.bit

5. When you have selected the above files, one last dialog will pop up. Simply click OK.

6. You now need to set the programming options. From the Edit menu select Preferences:



7. Select "Use HIGHZ instead of BYPASS" and click OK:



Congratulations! You have now completed initial setup of the iMPACT project. Be sure to save it.

To program a device, right-click on the device you wish to program and select Program. Click OK on the dialog that pops up, and you should see a blue "Program Succeeded" message.

The recommended programming sequence is to reprogram the slave FPGA(s) 1-3 as desired, and then re-program FPGA4 with the master bit file. The master [FPGA4] will re-load its control program from the FLASH PROM and you will then be able to reconnect to the VDFPGA board with the Falcon Client.

Technical explanation for the configuration changes and programming sequence:
Because there are multiple FPGAs connected to each other, the programming control pins of the FPGA in question may be driven to an incorrect value by its neighbor(s). Checking the HIGHZ option deactivates the other devices' output drivers, essentially isolating the device to be programmed.

However, this introduces a different problem. When the clock generator inside FPGA3 is disconnected, FPGA4 and all connected peripherals stop receiving clock signals and lose state. Thus, FPGA4 must always be reprogrammed last, both to restart the Microblaze processor and to reconfigure the peripherals.